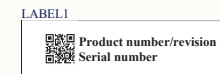
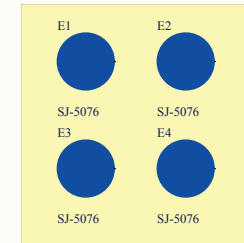
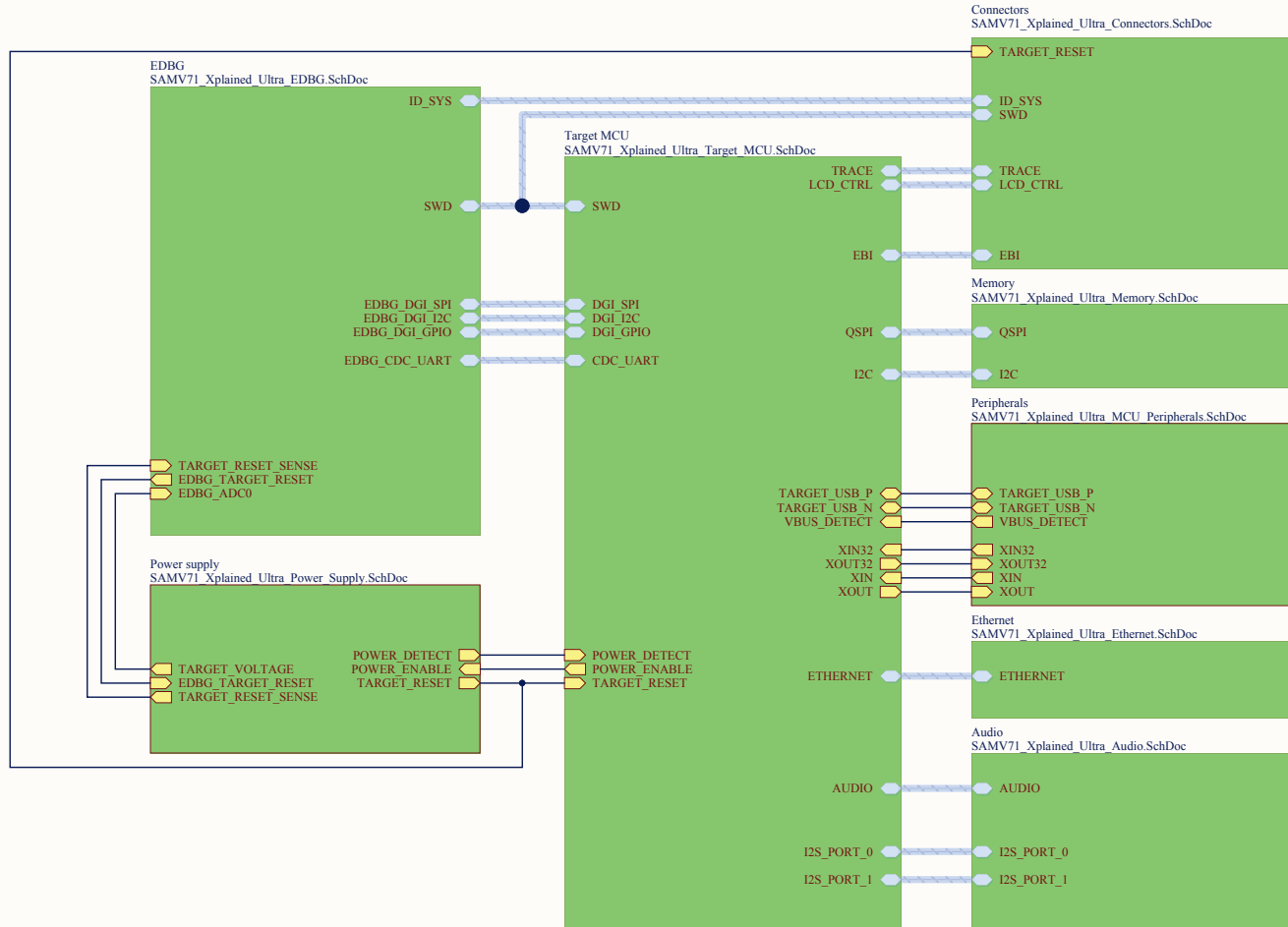


SAM V71 Xplained ULTRA

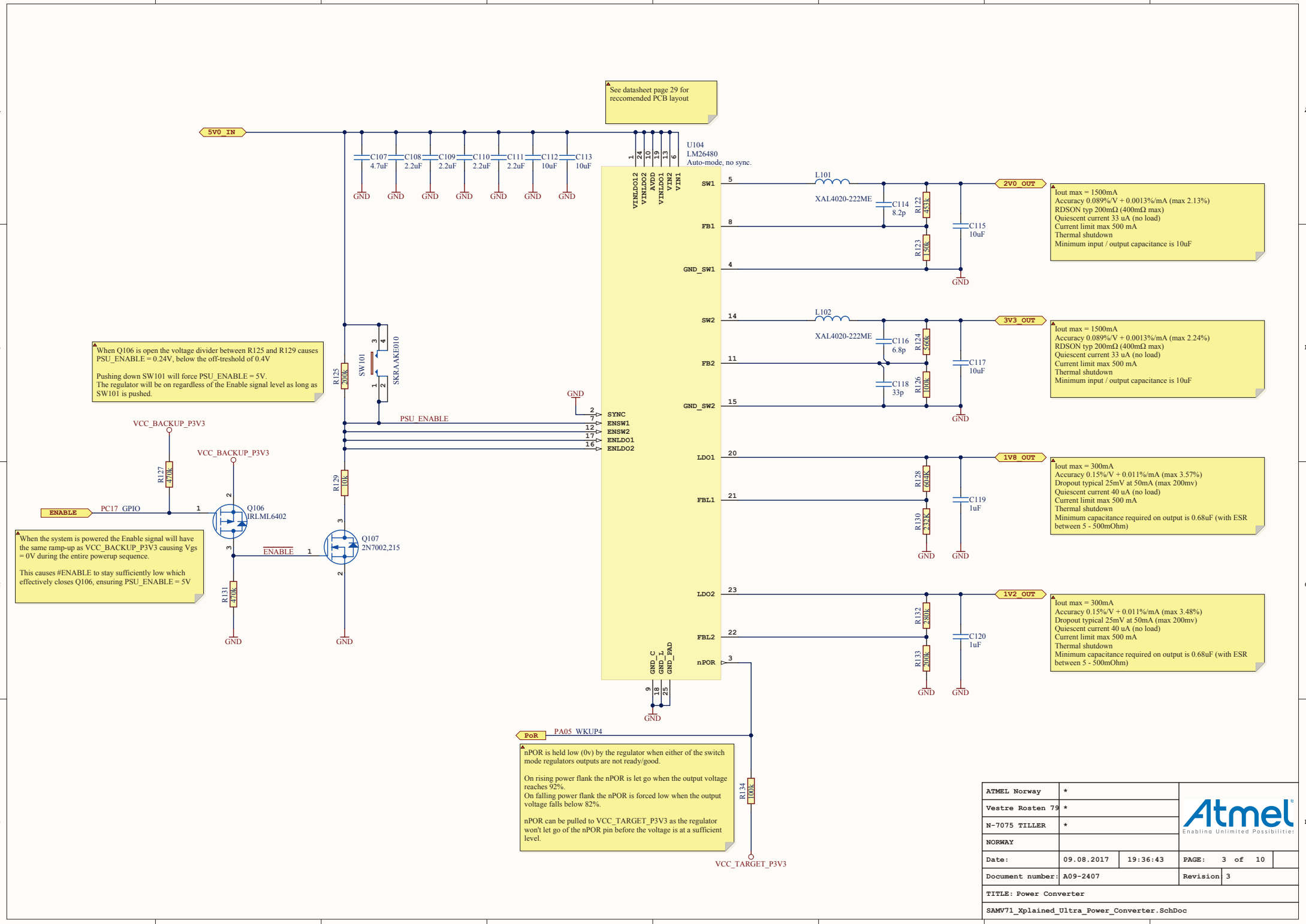


PCBA Label

PCB Documentation section showing PCB1, PCBADOC1, TESTDOC1, FW1, and TEST1 with their respective IDs and file names.

ATMEL Norway	*		
Vestre Rosten 79	*		
N-7075 TILLER	*		
NORWAY			
Date:	09.08.2017	19:36:42	PAGE: 1 of 10
Document number:	A09-2407		Revision 3
TITLE: Top Level Schematics			
SAMV71_Xplained_Ultra_TopLevel.SchDoc			





See datasheet page 29 for recommended PCB layout

When Q106 is open the voltage divider between R125 and R129 causes PSU_ENABLE = 0.24V, below the off-threshold of 0.4V
 Pushing down SW101 will force PSU_ENABLE = 5V. The regulator will be on regardless of the Enable signal level as long as SW101 is pushed.

When the system is powered the Enable signal will have the same ramp-up as VCC_BACKUP_P3V3 causing Vgs = 0V during the entire powerup sequence.
 This causes #ENABLE to stay sufficiently low which effectively closes Q106, ensuring PSU_ENABLE = 5V

I_{out} max = 1500mA
 Accuracy 0.089%/V + 0.0013%/mA (max 2.13%)
 RDS(on) typ 200mΩ (400mΩ max)
 Quiescent current 33 uA (no load)
 Current limit max 500 mA
 Thermal shutdown
 Minimum input / output capacitance is 10uF

I_{out} max = 1500mA
 Accuracy 0.089%/V + 0.0013%/mA (max 2.24%)
 RDS(on) typ 200mΩ (400mΩ max)
 Quiescent current 33 uA (no load)
 Current limit max 500 mA
 Thermal shutdown
 Minimum input / output capacitance is 10uF

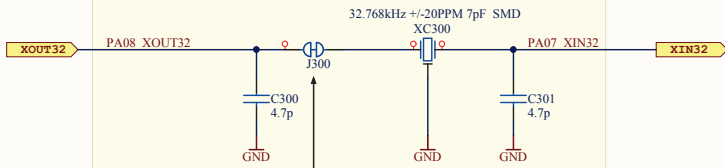
I_{out} max = 300mA
 Accuracy 0.15%/V + 0.011%/mA (max 3.57%)
 Dropout typical 25mV at 50mA (max 200mv)
 Quiescent current 40 uA (no load)
 Current limit max 500 mA
 Thermal shutdown
 Minimum capacitance required on output is 0.68uF (with ESR between 5 - 500mOhm)

I_{out} max = 300mA
 Accuracy 0.15%/V + 0.011%/mA (max 3.48%)
 Dropout typical 25mV at 50mA (max 200mv)
 Quiescent current 40 uA (no load)
 Current limit max 500 mA
 Thermal shutdown
 Minimum capacitance required on output is 0.68uF (with ESR between 5 - 500mOhm)

PoR PA05 WKUP4
 nPOR is held low (0v) by the regulator when either of the switch mode regulators outputs are not ready/good.
 On rising power flank the nPOR is let go when the output voltage reaches 92%.
 On falling power flank the nPOR is forced low when the output voltage falls below 82%.
 nPOR can be pulled to VCC_TARGET_P3V3 as the regulator won't let go of the nPOR pin before the voltage is at a sufficient level.

ATMEL Norway	*		
Vestre Rosten 79	*		
N-7075 TILLER	*		
NORWAY			
Date:	09.08.2017	19:36:43	PAGE: 3 of 10
Document number:	A09-2407	Revision	3
TITLE: Power Converter			
SAMV71_Xplained_Ultra_Power_Converter_SchDoc			

32.768 kHz Crystal



These straps with SMD pads can be used to place a resistor in the XOUT signal in order to measure the oscillator allowance.
By default these straps are closed and nothing is mounted on the pads.

Crystal datasheet:
Crystal = 7pF
max ESR = 60kOhm
Accuracy +20ppm

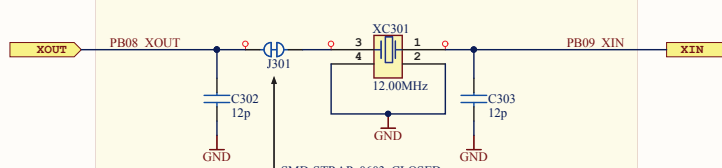
SAM V71 datasheet:
Cpara = 0.5pF (Typical)
max ESR = 100kOhm
PCB capacitance: Cpcb = 1pF (estimated)

Estimated load
C = 2 (Crystal - Cpara - Cpcb)
C = 2 (7pF - 0.5pF - 1pF)
C = 11pF

Selected in design
C = 10pF

Verification showed: 4.7pF
Accuracy: 5.2 ppm
Startup time: 400 ms to reach full swing with a 9.5pF probe connected to the crystal.
Safety factor: Above 5.5

12 MHz Crystal



These straps with SMD pads can be used to place a resistor in the XOUT signal in order to measure the oscillator allowance.
By default these straps are closed and nothing is mounted on the pads.

Crystal datasheet:
Crystal = 20pF
max ESR = 80 Ohm
Accuracy +20ppm

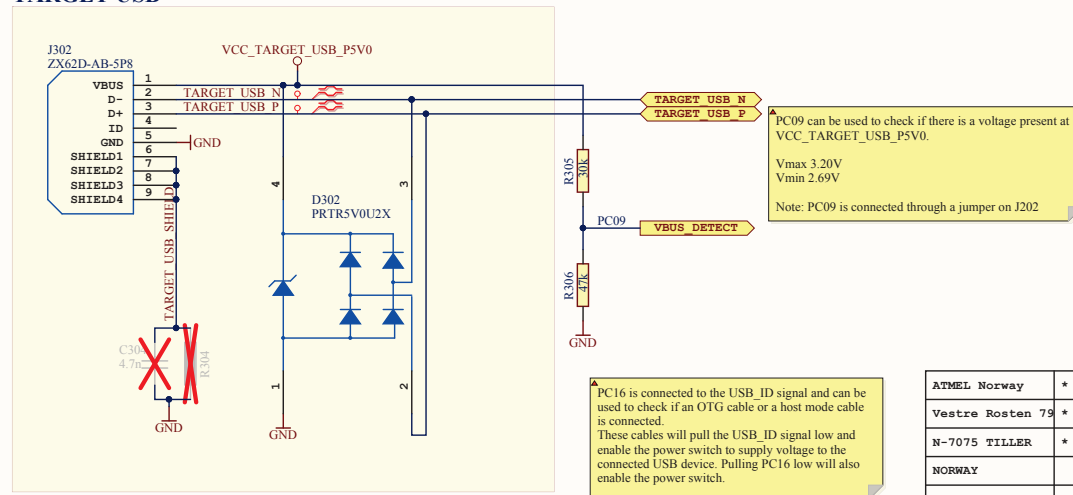
SAM V71 datasheet:
CL = 9.0pF (typical)
Maximum load 17.5pF
Maximum ESR = 100 Ohm
Estimated Cpcb = 1pF

C = 2 (Crystal - CL - Cpcb)
C = 2 (20pF - 9pF - 1pF)
C = 20pF

Selected in design
C = 18pF

Verification showed: 12.0pF
Accuracy 5 ppm
Startup: full swing after 850 μs (first clock after 451 μs)
Safety factor: Above 5.5


TARGET USB



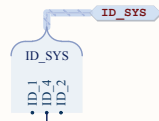
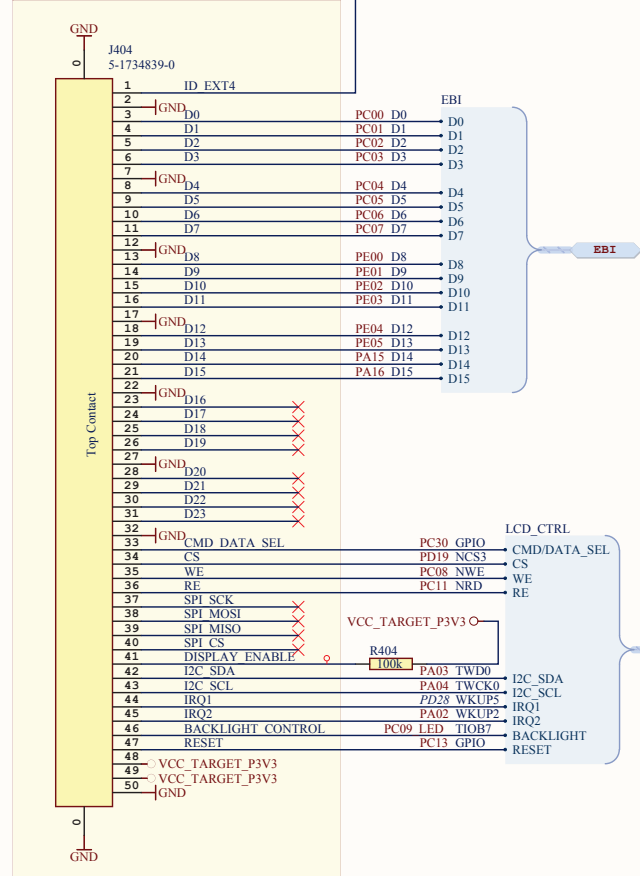
PC09 can be used to check if there is a voltage present at VCC_TARGET_USB_P5V0.
Vmax 3.20V
Vmin 2.69V
Note: PC09 is connected through a jumper on J202

PC16 is connected to the USB ID signal and can be used to check if an OTG cable or a host mode cable is connected.
These cables will pull the USB ID signal low and enable the power switch to supply voltage to the connected USB device. Pulling PC16 low will also enable the power switch.

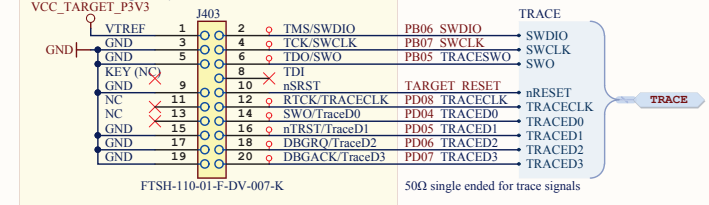
Since you do not plan to use USB HOST I removed USB ID parts
Also, since we removed power multiplexer, VCC_TARGET_USB_P5V0 - can not be used for board supply

ATMEL Norway	*	 Enabling Unlimited Possibilities			
Vestre Rosten 79	*				
N-7075 TILLER	*				
NORWAY		Date:	09.08.2017	19:36:43	PAGE: 5 of 10
Document number:		A09-2407		Revision 3	
TITLE: Target MCU Peripherals					
SAMV71_Xplained_Ultra_MCU_Peripherals_SchDoc					

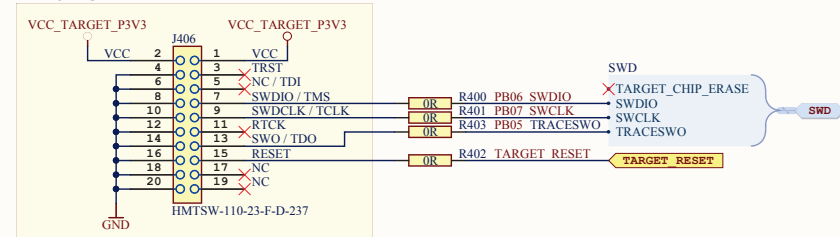
EXT4 LCD Connector



TRACE (CoreSight 20)

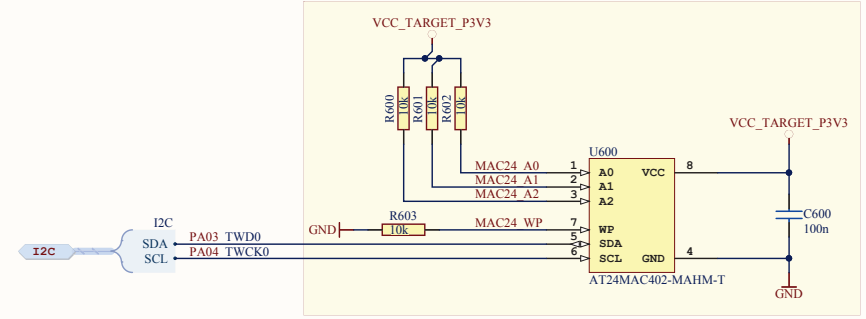


ARM JTAG

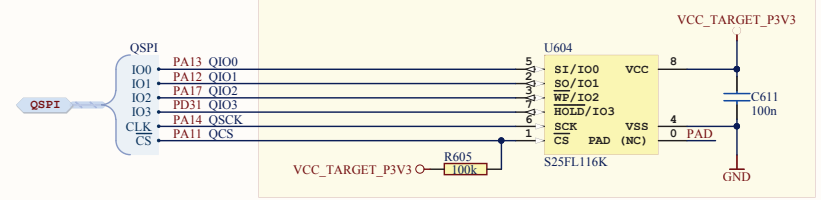


ATMEL Norway	*			<p>Enabling Unlimited Possibilities</p>
Vestre Rosten 79	*			
N-7075 TILLER	*			
NORWAY				
Date:	09.08.2017	19:36:43	PAGE:	6 of 10
Document number:	A09-2407		Revision	3
TITLE: Extension connectors				
SAMV71_Xplained_Ultra_Connectors_SchDoc				

Serial EEPROM with EIA-48 MAC address

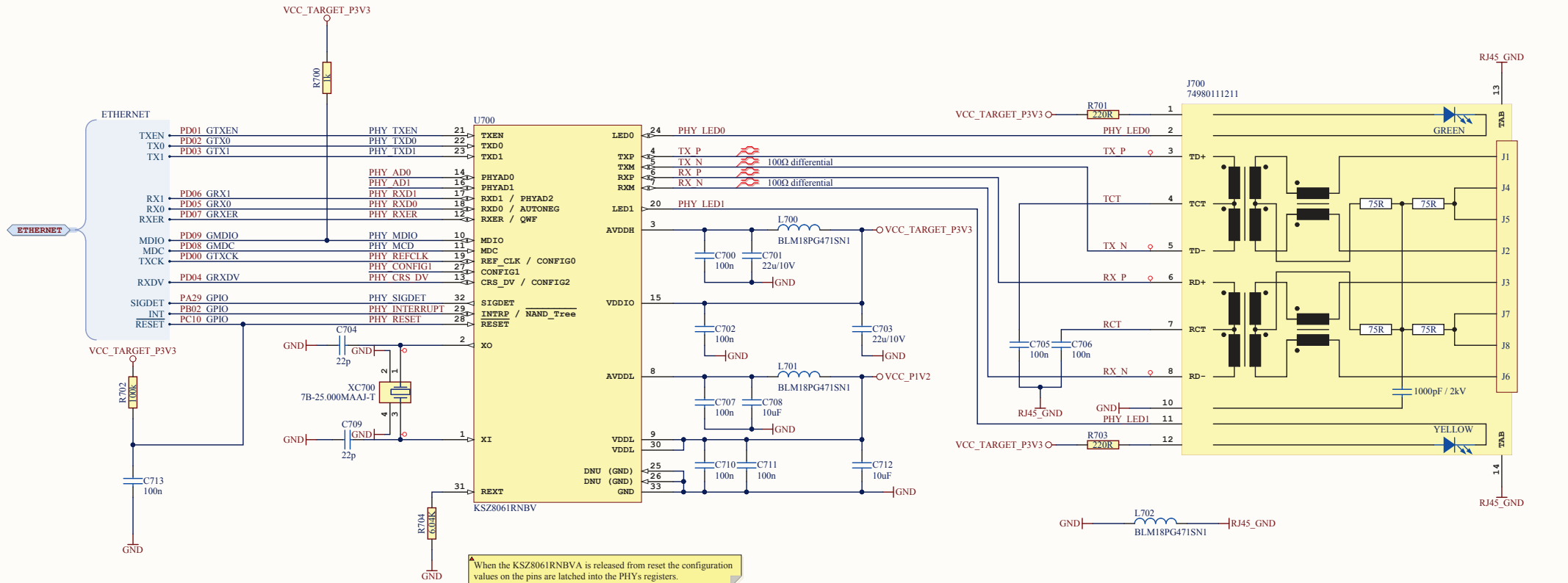


QSPI FLASH



ATMEL Norway	*		
Vestre Rosten 79	*		
N-7075 TILLER	*		
NORWAY			
Date:	09.08.2017	19:36:43	PAGE: 7 of 10
Document number:	A09-2407		Revision 3
TITLE: Memory			
SAMV71_Xplained_Ultra_Memory.SchDoc			





When the KSZ8061RNBVA is released from reset the configuration values on the pins are latched into the PHY's registers.

▲ PHYAD[2:0] is used to set the PHYs address:
001 (default on board)
010
...
110
111

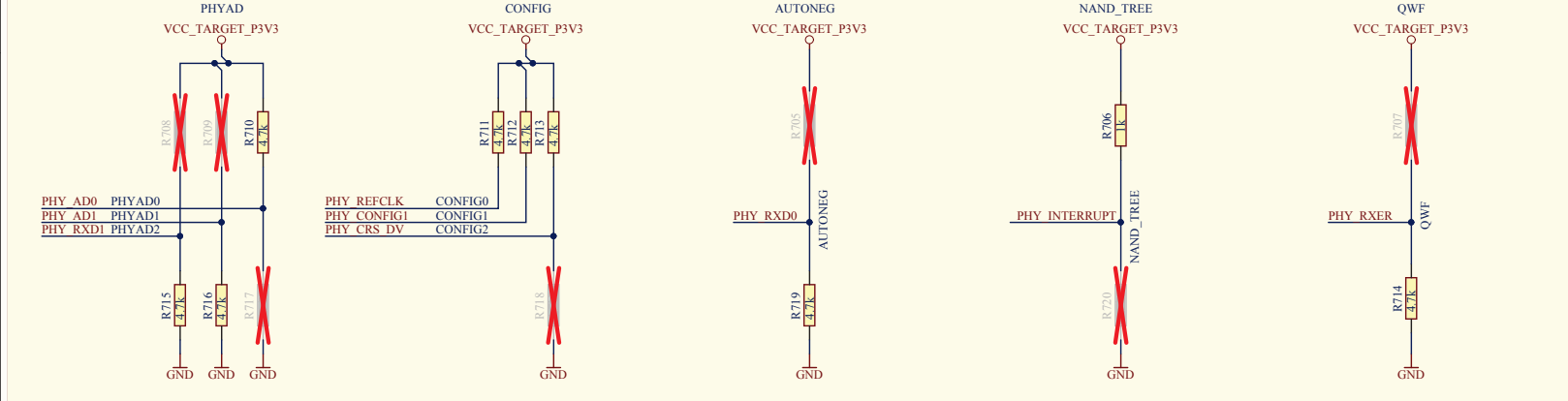
▲ CONFIG[2:0] is used to select operation mode:
001 = RMII normal, MDI/MDI-X disabled
101 = RMII back to back
111 = RMII normal MDI/MDI-X enabled
Not configurable on board as back to back

▲ AUTONEG is used to select if auto negotiation of link speed should be enabled.
1 = disable Auto-Negotiation
0 = enable Auto-Negotiation (default on board)

▲ NAND_TREE enables a test mode for all pins connected to the SAMV71Q21.
1 = Disable NAND_TREE (default on board)
0 = Enable NAND_TREE

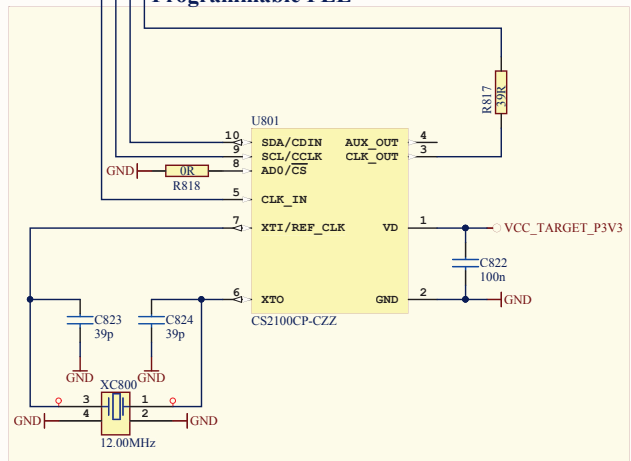
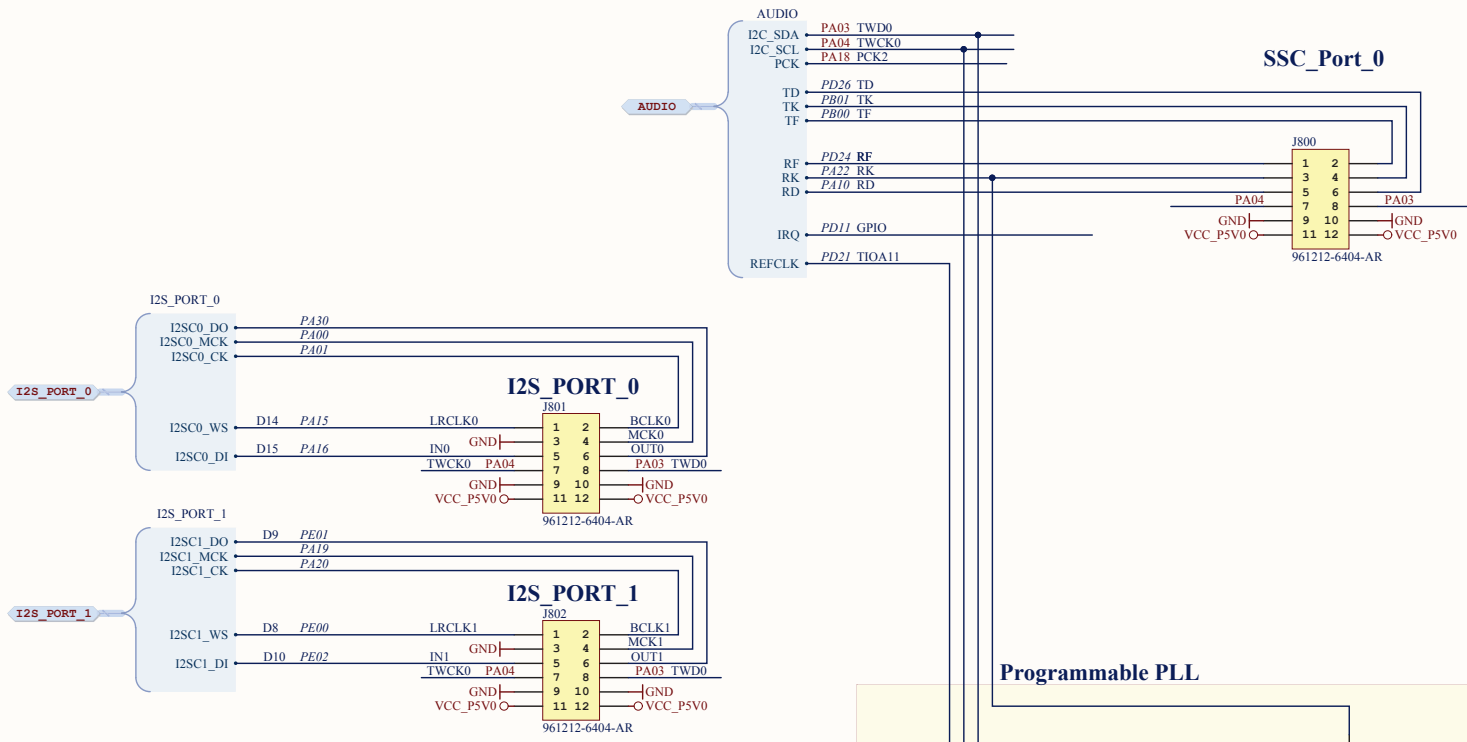
▲ QWF is used to enable/disable Quiet-WIRE Filtering
1 = Disale Quiet-WIRE Filtering
0 = Enable Quiet-WIRE Filtering (default on board)

PHY Configuration



ATMEL Norway	*		
Vestre Rosten 79	*		
N-7075 TILLER	*		
NORWAY			
Date:	09.08.2017	19:36:44	PAGE: 8 of 10
Document number:	A09-2407	Revision	3
TITLE: Ethernet			
SAMV71_Xplained_Ultra_Ethernet.SchDoc			

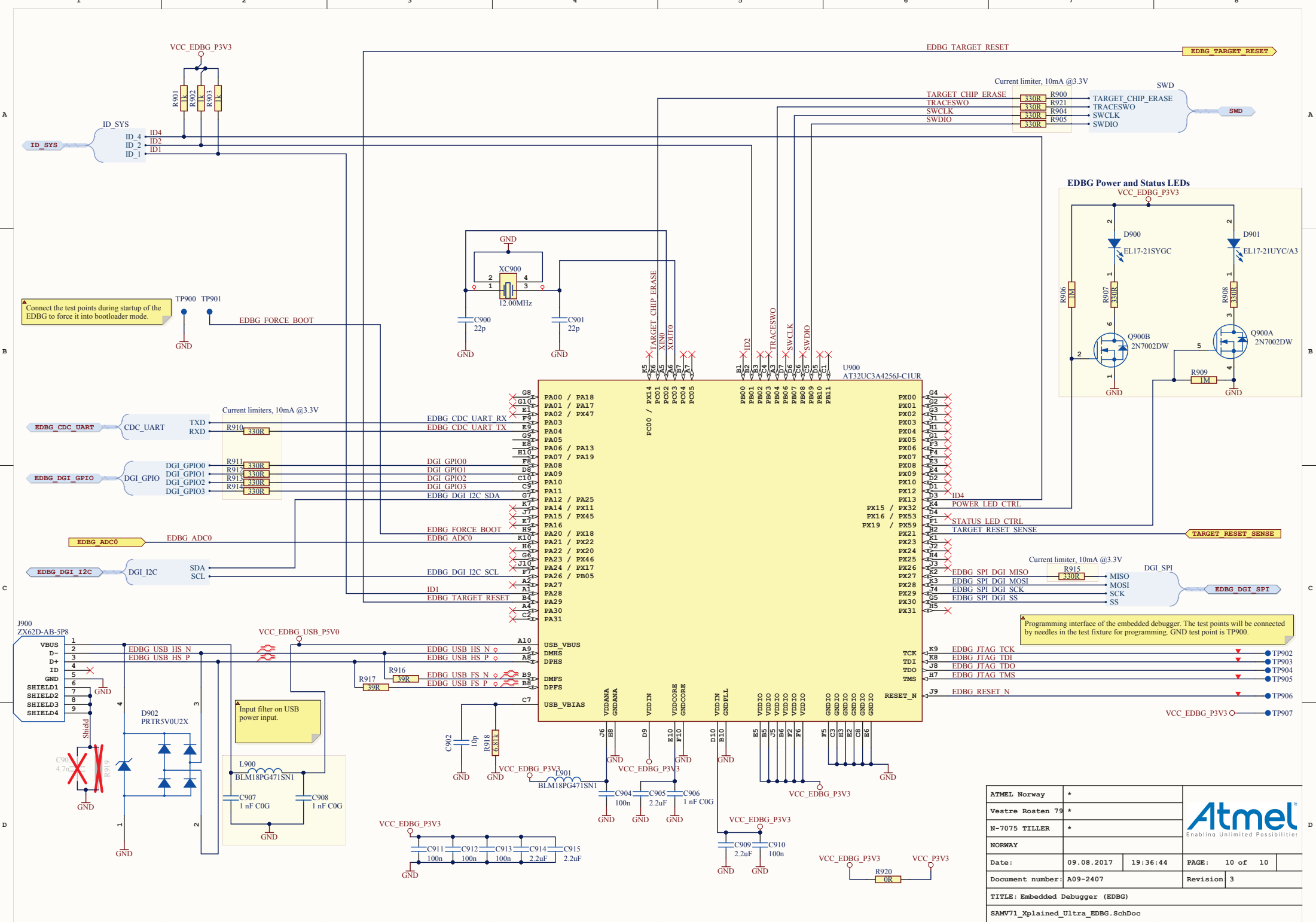




The external PLL is added specifically support Ethernet AVB applications. The timer output TIOA11 can be used to generate a reference clock which is connected to the PLL, the PLL can multiply this frequency to reconstruct a remote clock for the Audio system.

ATMEL Norway	*		
Vestre Rosten 79	*		
N-7075 TILLER	*		
NORWAY			
Date:	09.08.2017	19:36:44	PAGE: 9 of 10
Document number:	A09-2407	Revision	3
TITLE: Audio			
SAMV71_Xplained_Ultra_Audio.SchDoc			





Connect the test points during startup of the EDBG to force it into bootloader mode.

Input filter on USB power input.

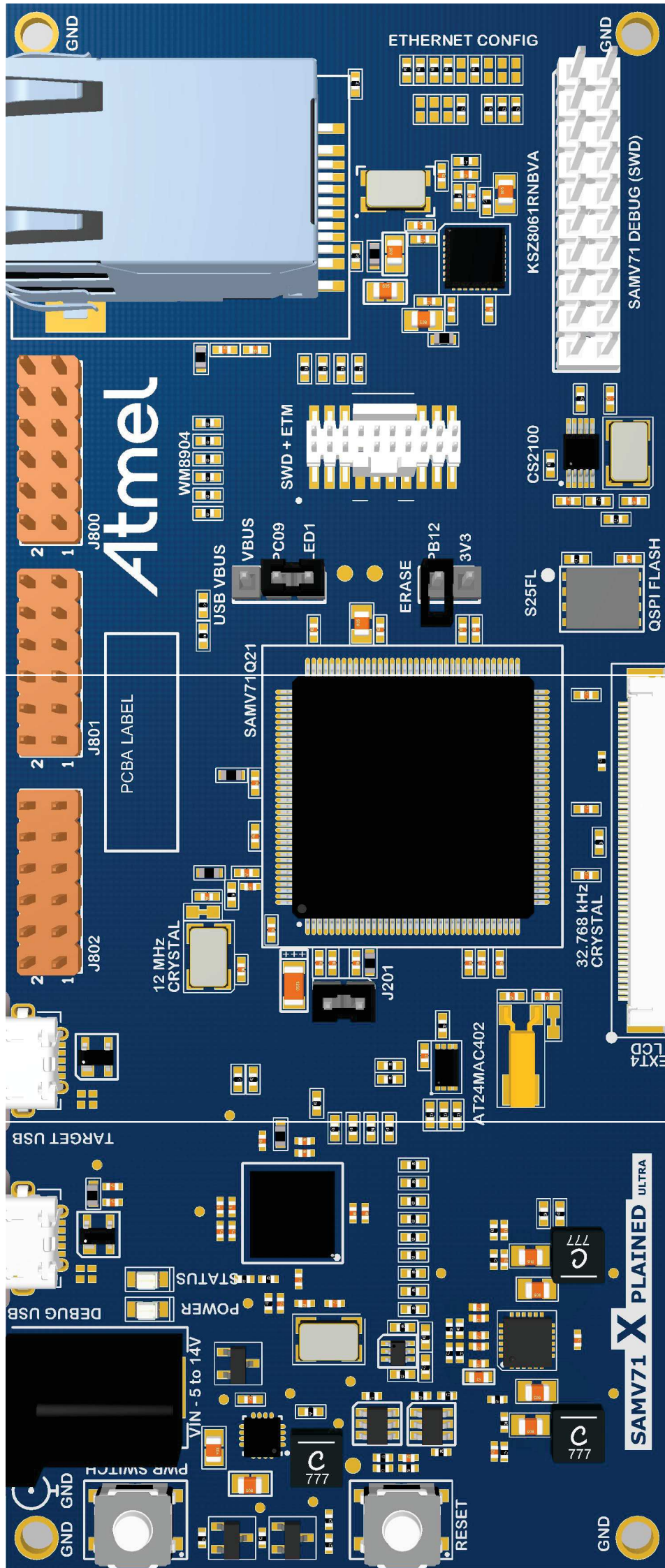
Programming interface of the embedded debugger. The test points will be connected by needles in the test fixture for programming. GND test point is TP900.

ATMEL Norway	*		
Vestre Rosten 79	*		
N-7075 TILLER	*		
NORWAY			
Date:	09.08.2017	19:36:44	PAGE: 10 of 10
Document number:	A09-2407		Revision 3
TITLE: Embedded Debugger (EDBG)			
SAMV71_Xplained_Ultra_EDBG_SchDoc			

EDBG TARGET RESET

TARGET RESET SENSE

VCC_EDBG_P3V3 O



Atmel

SAMV71 X PLAINED ULTRA

PCBA LABEL

ETHERNET CONFIG

GND

GND

TARGET USB

DEBUG USB

POWER

STATUS

PWR SWITCH

VIN - 5 to 14V

GND

RESET

GND

J800

J801

J802

J201

12 MHz CRYSTAL

32.768 kHz CRYSTAL

SAMV71Q21

WM8904

SWD + ETM

USB VBUS

VBUS

PC09

LED1

ERASE

DPB12

3V3

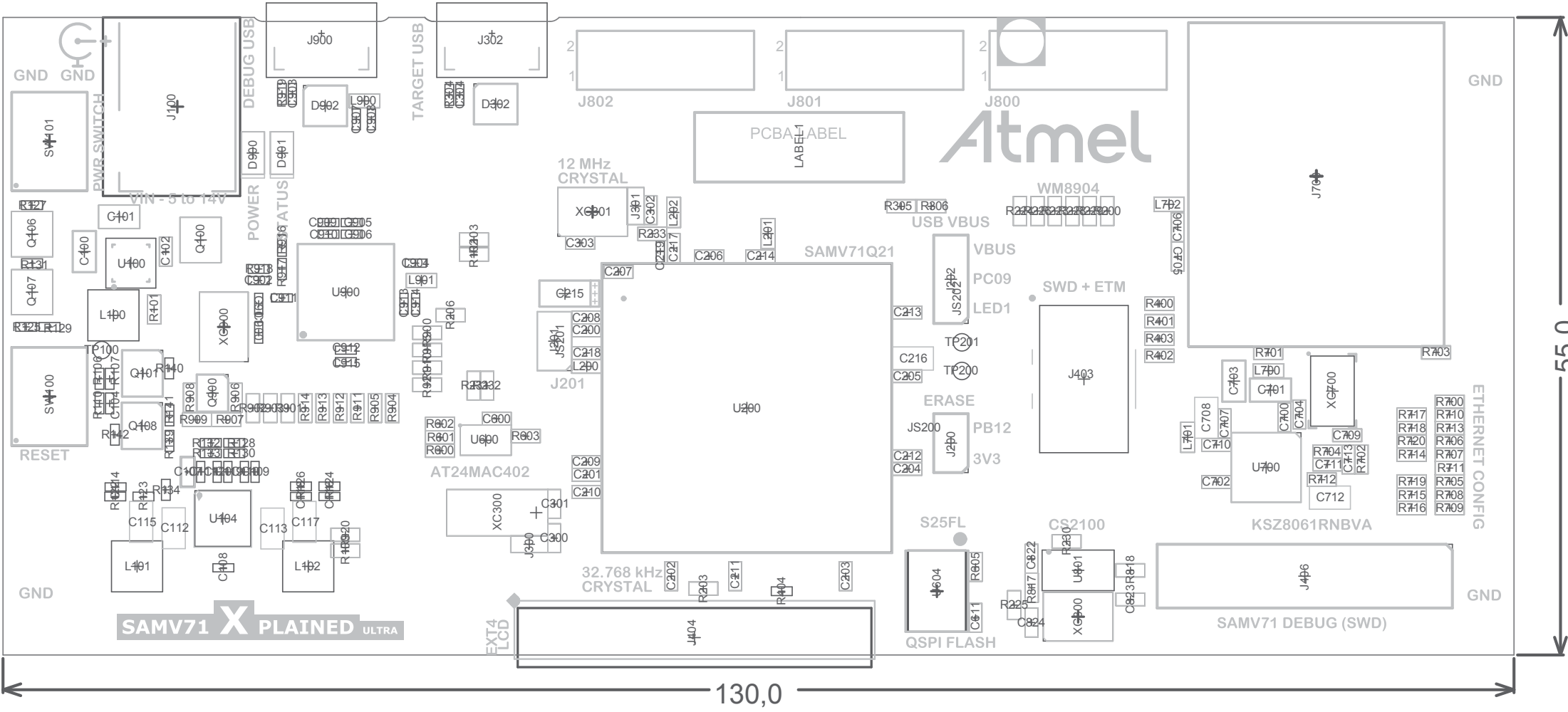
CS2100

S25FL

QSPI FLASH

KSZ8061RNBVA

SAMV71 DEBUG (SWD)



SAMV71 X PLAINED ULTRA

Atmel

PCBA LABEL-1

130,0

55,0

GND GND

GND

GND

GND

ETHERNET CONFIG

12 MHz CRYSTAL

32.768 kHz CRYSTAL

SAMV71Q21

WM8904

USB VBUS

SWD + ETM

ERASE

S25FL

QSPI FLASH

KSZ8061RNBVA

SAMV71 DEBUG (SWD)

SW401

RESET

GND

TARGET USB

J802

J801

J800

PCBA LABEL-1

X401

J201

U400

SAMV71Q21

USB VBUS

SWD + ETM

ERASE

S25FL

QSPI FLASH

KSZ8061RNBVA

SAMV71 DEBUG (SWD)

SW401

RESET

GND

TARGET USB

J802

J801

J800

PCBA LABEL-1

X401

J201

U400

SAMV71Q21

USB VBUS

SWD + ETM

ERASE

S25FL

QSPI FLASH

KSZ8061RNBVA

SAMV71 DEBUG (SWD)

SW401

RESET

GND

TARGET USB

J802

J801

J800

PCBA LABEL-1

X401

J201

U400

SAMV71Q21

USB VBUS

SWD + ETM

ERASE

S25FL

QSPI FLASH

KSZ8061RNBVA

SAMV71 DEBUG (SWD)

SW401

RESET

GND

TARGET USB

J802

J801

J800

PCBA LABEL-1

X401

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U400

SAMV71Q21

USB VBUS

SWD + ETM

ERASE

S25FL

QSPI FLASH

KSZ8061RNBVA

SAMV71 DEBUG (SWD)

SW401

RESET

GND

TARGET USB

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PCBA LABEL-1

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U400

SAMV71Q21

USB VBUS

SWD + ETM

ERASE

S25FL

QSPI FLASH

KSZ8061RNBVA

SAMV71 DEBUG (SWD)

SW401

RESET

GND

TARGET USB

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PCBA LABEL-1

X401

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U400

SAMV71Q21

USB VBUS

SWD + ETM

ERASE

S25FL

QSPI FLASH

KSZ8061RNBVA

SAMV71 DEBUG (SWD)

SW401

RESET

GND

TARGET USB

J802

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J800

PCBA LABEL-1

X401

J201

U400

SAMV71Q21

USB VBUS

SWD + ETM

ERASE

S25FL

QSPI FLASH

KSZ8061RNBVA

SAMV71 DEBUG (SWD)

SW401

RESET

GND

TARGET USB

J802

J801

J800

PCBA LABEL-1

X401

J201

U400

SAMV71Q21

USB VBUS

SWD + ETM

ERASE

S25FL

QSPI FLASH

KSZ8061RNBVA

SAMV71 DEBUG (SWD)

SW401

RESET

GND

TARGET USB

J802

J801

J800

PCBA LABEL-1

X401

J201

U400

SAMV71Q21

USB VBUS

SWD + ETM

ERASE

S25FL

QSPI FLASH

KSZ8061RNBVA

SAMV71 DEBUG (SWD)

SW401

RESET

GND

TARGET USB

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PCBA LABEL-1

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SAMV71Q21

USB VBUS

SWD + ETM

ERASE

S25FL

QSPI FLASH

KSZ8061RNBVA

SAMV71 DEBUG (SWD)

SW401

RESET

GND

TARGET USB

J802

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J800

PCBA LABEL-1

X401

J201

U400

SAMV71Q21

USB VBUS

SWD + ETM

ERASE

S25FL

QSPI FLASH

KSZ8061RNBVA

SAMV71 DEBUG (SWD)

SW401

RESET

GND

TARGET USB

J802

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J800

PCBA LABEL-1

X401

J201

U400

SAMV71Q21

USB VBUS

SWD + ETM

ERASE

S25FL

QSPI FLASH

KSZ8061RNBVA

SAMV71 DEBUG (SWD)

SW401

RESET

GND

TARGET USB

J802

J801

J800

PCBA LABEL-1

X401

J201

U400

SAMV71Q21

USB VBUS

SWD + ETM

ERASE

S25FL

QSPI FLASH

KSZ8061RNBVA

SAMV71 DEBUG (SWD)

SW401

RESET

GND

TARGET USB

J802

J801

J800

PCBA LABEL-1

X401

J201

U400

SAMV71Q21

USB VBUS

SWD + ETM

ERASE

S25FL

QSPI FLASH

KSZ8061RNBVA

SAMV71 DEBUG (SWD)

SW401

RESET

GND

TARGET USB

J802

J801

J800

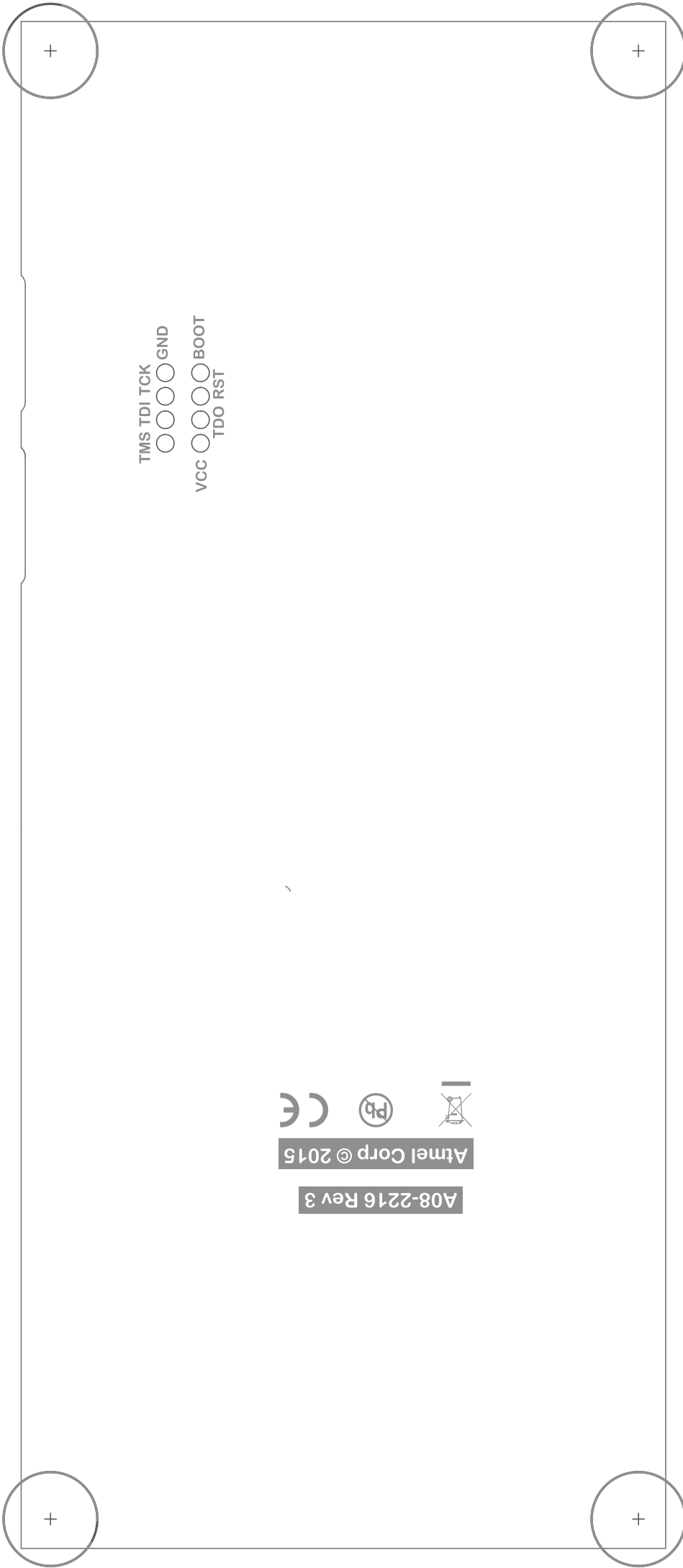
PCBA LABEL-1

X401

J201

U400

SAMV71Q21



+

+

TMS TDI TCK
○ ○ ○ ○ GND
VCC ○ ○ ○ ○ BOOT
TDO RST

A08-2216 Rev 3
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RoHS Pb CE

+

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